LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for manufacturing a semiconductor device comprising:

providing a semiconductor die of a semiconductive material having a channel receiving layer of a first conductivity;

forming a layer of oxidation retardant material over said channel receiving layer;

removing a portion of said oxidation retardant material to expose said semiconductor die;

etching said exposed semiconductor die to form a termination recess around said oxidation retardant material remaining after said receiving step, said termination recess including a sidewall and a bottom;

forming an oxide on said sidewall and said bottom of said termination recess; and

forming trenches in said channel receiving layer ~~in one region of said channel receiving layer;~~

~~forming a termination recess around said trenches said termination recess having exposed surfaces of semiconductive material;~~ after forming said oxide on said sidewall and said bottom of said termination recess.

~~forming another layer of oxidation retardant material over sidewalls and bottom of each of said trenches; and~~

~~growing an oxide layer on exposed surfaces of said termination recess.~~

2. (Original) A method according to claim 1, further comprising implanting channel dopants of a second conductivity in said channel receiving layer before forming said layer of oxidation retardant material; and diffusing said channel dopants after forming said layer of oxidation retardant material to form a channel region.

3. (Currently Amended) A method for manufacturing a semiconductor device comprising:

providing a semiconductor die of a semiconductive material having a channel receiving layer of a first conductivity;

forming a layer of oxidation retardant material over said channel receiving layer;

forming trenches in said channel receiving layer in one region of said channel receiving layer;

forming a termination recess around said trenches said termination recess having exposed surfaces of semiconductive material;

forming another layer of oxidation retardant material over sidewalls and bottom of each of said trenches;

growing an oxide layer on exposed surfaces of said termination recess;

implanting channel dopants of a second conductivity in said channel receiving layer before forming said layer of oxidation retardant material; and diffusing said channel dopants after forming said layer of oxidation retardant material to form a channel region;

~~A method according to claim 2, further comprising~~ removing oxidation retardant material from bottoms of said trenches leaving oxidation retardant material on said sidewalls of said trenches; forming a bottom oxide layer at said bottom of said trenches; removing said oxidation retardant material from said sidewalls of said trenches; and forming a layer of gate oxide on said sidewalls of said trenches; wherein said bottom oxide layer is thicker than said gate oxide layer.

4. (Original) A method according to claim 3, further comprising forming a gate electrode in each of said trenches; forming an insulation layer over said gate electrodes; and implanting dopants of said first conductivity in said channel region.

5. (Original) A method according to claim 4, wherein said gate electrodes are formed by depositing a layer of gate electrode material to at least fill said trenches and extend over said oxide layer in said termination recess; removing said gate electrode material to leave gate

electrode material only in the interior of said trenches without removing gate electrode material disposed over said termination recess.

6. (Original) A method according to claim 4, further comprising forming a layer of low temperature oxide over said trenches and said termination recess; patterning said layer of low temperature oxide with openings that extend to said semiconductor die and leaving low temperature oxide over said gate electrodes; and driving said dopants of said first conductivity to form conductive regions of said first conductivity adjacent said trenches.

7. (Original) A method according to claim 6, wherein said patterning includes forming a mask having mask openings over said low temperature oxide to identify regions in said low temperature oxide which will be removed to form openings in said low temperature oxide; and comprising laterally removing portions of said low temperature oxide below said mask openings and then vertically removing low temperature oxide to create said openings, whereby said openings in said low temperature oxide will be narrower adjacent said semiconductor die.

8. (Original) A method according to claim 6, further comprising forming a contact layer that extends to and makes electrical contact with said conductive regions of said first conductivity adjacent said trenches.

9. (Original) A method according to claim 6, wherein said openings expose said channel region.

10. (Original) A method according to claim 9, further comprising implanting dopants of said second conductivity type in said channel region exposed by said openings to increase the concentration of dopants thereof.

11. (Original) A method according to claim 9, further comprising removing a portion of said semiconductor die at the bottom of each opening to create depression that exposed said channel region.

12. (Original) A method according to claim 11, further comprising implanting dopants of said second conductivity type in said channel region exposed by said openings to increase the concentration of dopants thereof.

13. (Original) A method according to claim 1, wherein said oxidation retardant material is a nitride.

14. (Original) A method according to claim 1, wherein said channel receiving layer is an epitaxial layer of first conductivity formed over a monolithic substrate of said first conductivity.

15. (Original) A method according to claim 1, wherein said semiconductor device is a MOSFET.

16. (Currently Amended) A method for manufacturing a MOSgated semiconductor switching device, comprising:

providing a semiconductor die having a channel receiving region of first conductivity;

forming a channel region of second conductivity in said channel receiving region;

forming at least one trench in said semiconductor die extending through said channel region;

forming a gate structure in said at least one trench; and

forming a conductive region of said first conductivity type adjacent each side of said trench in said channel region after forming said gate structure; and

forming a low temperature oxide body over all of said gate structure, and at least a portion of said conductive region; and

forming recesses on a top portion of said low temperature oxide body.

17. (Original) A method according to claim 16, wherein said forming said conductive region comprises implanting dopants of said first conductivity in said channel region; applying a contact mask for forming a metal contact over said semiconductor die to serve as external connection for said conductive region; etching a depression through said conductive region to reach said channel region using said mask; implanting dopants of said second conductivity at the bottom of said depression, and diffusing said dopants of said first conductivity in a diffusion drive to form said conductive regions.

18. (Original) A method according to claim 16, further comprising forming a layer of oxidation retardant material on said sidewalls of said at least one trench, and forming a thick oxide at the bottom of said trench.

19. (Original) A method according to claim 16, further comprising forming a termination structure in said semiconductor die, said termination structure including a recess formed in said semiconductor die.

20. (Original) A method according to claim 16, wherein said gate structure includes a gate electrode insulated from said trench sidewalls by an insulation layer, wherein said insulation layer is formed by thermal oxidation before forming said conductive regions.